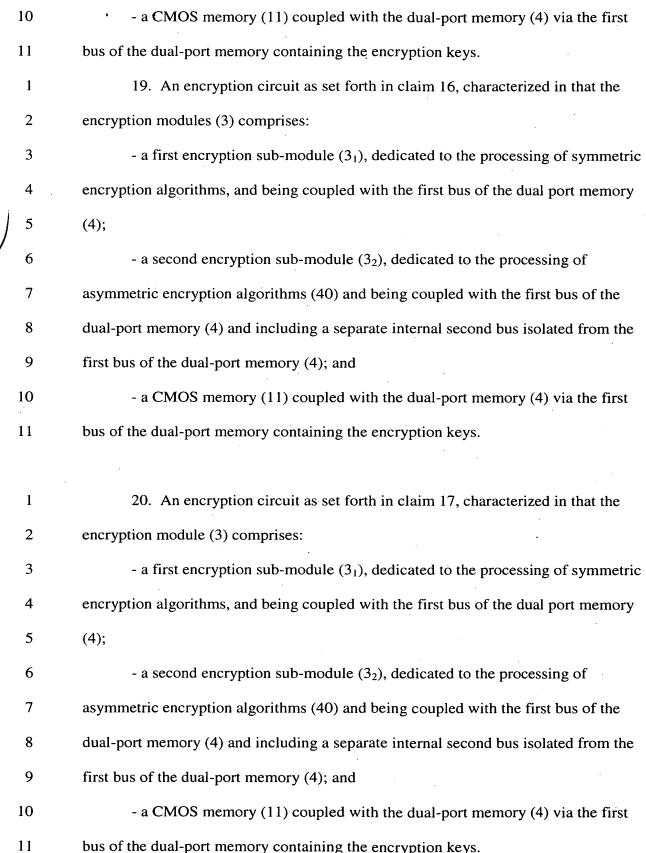


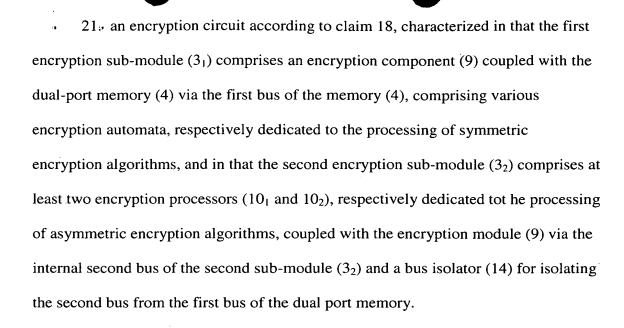


16. An encryption circuit according to claim 15, characterized in that the isolation means (4) of the circuit (1) comprises a double-port memory (4).

17. An encryption circuit according to claim 15 wherein this isolation means (4) comprises a double port memory coupled between the input/output module (2) and the encryption module (3), the dual-port memory (4) being coupled to a first bus and adapted to simultaneously handle the exchange of data, commands and statuses' between the input/output and encryption modules (2 and 3), and isolation between the two modules (2 and 3).

- 18. An encryption circuit is set forth in claim 15, characterized in that the encryption module (3) comprises:
- a first encryption sub-module (3<sub>1</sub>), dedicated to the processing of symmetric encryption algorithms, and being coupled with the first bus of the dual port memory (4);
- a second encryption sub-module (3<sub>2</sub>), dedicated to the processing of asymmetric encryption algorithms (40) and being coupled with the first bus of the dual-port memory (4) and including a separate internal second bus isolated from the first bus of the dual-port memory (4); and





- 22. An encryption circuit according to claim 21, characterized in that the encryption processors (10<sub>1</sub> and 10<sub>2</sub>) of the encryption module (30 are of the CIP type.
- 23. An encryption circuit according to claim 21, characterized in that one  $(10_1)$  of the two encryption processors  $(10_1$  and  $10_2)$  is of the CIP type, and in that the other  $(10_2)$  of the two encryption processors is of the ACE type.
- 24. An encryption circuit according to claim 21, characterized in that one of the two encryption processor (10<sub>2</sub>) is of the ACE type comprising a field programmable gate array (FPGA).
- 25. An encryption circuit according to claim 24, characterized in that the encryption component (9) is of the SCE type.

